Lesson Plan

Name of Faculty : Rahul Kaushik
Discipline : Computer Engg.
Semester : 3rd Sem
Subject : Digital Electronics
Lesson Plan Duration : 15 Weeks

Week	Theory		Practical	
	Lecture Day	Topic	Pr Day	Topic
1	1	Introduction a) Define digital and analog signals and systems, difference between analog and digital signals	1	Study of logic breadboard with verification of truth table for AND, OR, NOT, NAND, EX-OR, NOR gate
	2	b) Need of digitization and applications of digital systems		
	3	Number Systems a) Decimal, binary, octal, hexadecimal number systems		
2	4	b) Conversion of number from one number system to another including decimal points	2	Verification of NAND and NOR gate as universal gates
	5	c) Binary addition, subtraction, multiplication, division,		
	6	1's and 2's complement method of subtraction d) BCD code numbers and their limitations,		
3	7	addition of BCD coded numbers, conversion of BCD to decimal and vice-versa	3	Construction of half-adder and full adder circuits using EX-OR and NAND gate and verification of their operation
	8	e) Excess-3 code, gray code, binary to gray and gray to binary conversion		
	9	f) Concept of parity, single and double parity, error detection and correction using parity		
4	10	Revision	4	Verify the operation of a) multiplexer using an IC
	11	Logic Gates a) Logic gates, positive and negative logic, pulse waveform, definition,		
	12	symbols, truth tables, pulsed operation of NOT, OR, AND, NAND,		
5	13	NOR, EX-OR, EX-NOR gates	5	b)de-multiplexer

	14	b) NAND and NOR as universal logic gates		using an IC
	15	Revision		
6	16	Logic Simplification) a) Rules and laws of Boolean algebra, logic expression,	6	Revision
	17	Demorgan theorems, their proof b) Sum of products form (minterm), Product of sum form (maxterms),		
	18	simplification of Boolean expressions with the help of Rules and laws of Boolean algebra		
7	19	c) Karnaugh mapping techniques upto 4 variables and their applications for simplification of Boolean expression	7	Verify the operation of BCD to decimal decoder using an IC
	20	Arithmetic Circuits a) Half adder, full adder circuits and their operation		
	21	b) Parallel binary adder, 2-bit and 4-bit binary full adder, block diagram, working		
8	22	Revision	8	Verify the operation of BCD to 7 segment decoder using an IC
	23	Multiplexer/Demultiplexer a) Basic functions, symbols and logic diagrams of 4-inputs and 8-inputs multiplexers,		
	24	b) Function/utility of 16 and 32 inputs multiplexers,		
9	25	c) Realization of Boolean expression using multiplexer/demultiplexers	9	Verify operation of SR, JK, D-flip-flop master slave JK filp-flop using IC
	26	Revision		
	27	Decoders, Display Devices and Associated Circuits		
10	28	a) Basic Binary decoder, 4-line to 16 line decoder circuit	10	Revision

	29	b) BCD to decimal decoder, BCD to 7-segment decoder/driver, LED/LCD display		
	30	Revision		
11	31	Encoders and Comparators a) Encoder, decimal to BCD encoder,	11	Verify operation of SISO, PISO, SIPO, PIPO shift register. (universal shift register)
	32	decimal to BCD priority encoder, keyboard encoder		
	33	b) Magnitude comparators, symbols and logic diagrams of 2-bit and 4-bit, c) Comparators		
12	34	Latches and Flip-Flops a) Latch, SR-latch, D-latch, Flip-flop, difference between latch and flip-flop	12	Study of ring counter, Up/down counter
	35	b) S-R, D flip-flop their operation using waveform and truth tables, race around condition		
	36	c) JK flip-flop, master slave and their operation using waveform and truth tables		
13	37	Revision	13	Construct and verify the operation of an asynchronous binary decade counter using JK flip-flop
	38	Counters a) Asynchronous counter, 4-bit Asynchronous counter, Asynchronous decade counter		
	39	b) Asynchronous counter, 4-bit synchronous binary counter, Asynchronous decade counter		
14	40	c) Up/down Asynchronous counters, divide by N counter	14	Testing of digital ICs using IC tester
	41	MOD-3,MOD-5, MOD-7, MOD-12 counters d) Ring counter, cascaded counter, counter applications		
	42	Shift Registers a) Shift registers functions, serial-in-serial out,		
15	43	serial-in-parallel-out, parallel-in-serial-out, parallel-in-parallel out	15	Revision
	44	b) Universal shift register, shift register counter and		
	45	applications of shift registers		